UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/824,219	04/13/2004	Shumpei Kawasaki	101-9409J	6297

7590 01/27/2006

Alan R. Loudermilk
Loudermilk & Associates
P.O. Box 3607
Los Altos, CA 94024-0607

EXAMINER	
EL HADY, NABIL M	
ART UNIT	**PAPER NUMBER**
2152	

DATE MAILED: 01/27/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/824,219	KAWASAKI ET AL.	
	Examiner	Art Unit	
	Nabil M. El-Hady	2152	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *28 December 2005*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *17-22* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *17-22* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☒ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

1. Claims 1-22 are pending in this application. Claims 1-16 are cancelled. Claim 17 is amended. Claims 17-22 are presented for examination.

2. The text of those sections of Title 35, U.S. Code not included in this action can be found in a prior Office action.

3. Claims 17-22 are rejected under 35 U.S.C. 102(e) as being anticipated by Uchiyama et al. (USPN 5,574,876), hereafter "Uchiyama".

The applied reference has a common assignee with the instant application. Based upon the earlier effective U.S. filing date of the reference, it constitutes prior art under 35 U.S.C. 102(e). This rejection under 35 U.S.C. 102(e) might be overcome either by a showing under 37 CFR 1.132 that any invention disclosed but not claimed in the reference was derived from the inventor of this application and is thus not the invention "by another," or by an appropriate showing under 37 CFR 1.131.

4. As to claim 17, Uchiyama discloses the invention as claimed including a data processor comprising a central processing unit executing a plurality of instructions (MPU 101, Fig. 2), a clock pulse generator generating a plurality of clock signals (CG 103, and signals 150, 151, and 152, Fig. 1), a mode register accessed by the central processing unit (CMR 505, Fig. 5A; and col. 5, lines 58-59), wherein the data processor operates in accordance with a plurality of operation modes (abstract), wherein the central processing unit executes instructions and receives a clock signal from the clock pulse generator in a first mode of operation (col. 4, lines 56-61; and 150 clock signal, Fig. 1), wherein the central processing unit halts executing the

instructions and the clock pulse generator generates clock signals in another mode of operation (col. 4, lines 28-40; and col. 5, lines 58-64), and wherein the central processing unit and the clock pulse generator halt operation in one mode of operation (col. 4, lines 28-40; col. 5, lines 58-64; and col. 9, lines 14-21).

5. As to claim 18, Uchiyama discloses a control terminal receiving a level signal for the data processor to change operation (104, Fig. 7).

6. As to claim 19, Uchiyama discloses an external interrupt receive terminal which receives an interrupt request from outside the data processor in order to change the operation mode of the data processor (col. 5, lines 60-64).

7. As to claim 20, Uchiyama discloses a reset terminal, which receives a signal from outside the data processor in order to change the operation mode of the data processor (col. 5, lines 60-64).

8. As to claim 21, Uchiyama discloses halting providing a generated clock signal to the central processing unit in one mode of operation (inherent in col. 4, lines 28-40).

9. As to claim 22, Uchiyama discloses a data transfer controller that controls data transfer between the data processor and outside of the data processor (MS CONTROL UNIT 704 of Fig. 7 as part of MC CORE 104, Fig. 12, controlling data transfer between MPU CORE 101 and outside MS 102), and the clock pulse generator provides a clock signal to the central processing

unit and halts providing clock signal to the data transfer controller in one mode of operation (col. 9, lines 16-17).

10. Applicant's arguments filed 12/28/2005 have been fully considered but they are not persuasive. Rejection to claims 17-22 is maintained.

11. In the remarks, applicants argued in substance that the mode register provided by Uchiyama does not control the operation of the MPU; rather it controls the operation of the synchronous DRAM. Examiner respectfully traverses applicants' remarks.

12. First, Uchiyama discloses that control signals for the dynamic memory must be prepared on the basis of the system clock of the processor system (col. 1, lines 48-51). The processor and the synchronous memory must have compatibility with a wide range of applications (col. 2, lines 28-32), The memory is a synchronous dynamic memory which operates in synchronism with a clock signal applied to its clock input terminal (col. 3, lines 17-19). Individual components of the processor system operate in synchronism with a single system clock (col. 4, lines 37-39). It is clear that the operation mode of the chip 501 of Uchiyama represents also an operation mode for the MPU because it operates in synchronism with the MPU, i.e. the operation mode of the MPU is substantially based on the mode setting for the synchronous dynamic memory as claimed.

13. Second, the concept of a data processor operating in accordance with a plurality of operation modes based on a mode register is not new in the art, as shown in the following rejection.

14. Claim 17 is rejected under 35 U.S.C. 103(a) as being unpatentable over Akatsuka (US 4,589,020).

15. Akatsuka discloses a data processor executing a plurality of instructions (CPU 14, Fig. 3), a clock pulse generator generating a plurality of clock signals (16 and 17, Fig. 3), a mode register accessed by the central processing unit (18, Fig. 3), wherein the data processor operates in accordance with a plurality of operation modes based on the mode register (col. 5, lines 5-10), wherein the central processing unit executes instructions and receives a clock signal from the clock pulse generator in a first mode of operation (col. 5, lines 14-17), wherein the central processing unit halts executing the instructions and the clock pulse generator generates clock signals in another mode of operation (col. 4, line 66 to col. 5, line 4).

16. Akatsuka may not disclose the third mode of operation, that is the central processing unit and the clock pulse generator halt operation in one mode of operation. However, it would have been obvious to one skilled in the art at the time of the invention that having the concept of a mode register to control the operations of the CPU, and demonstrating the use of the concept through the first and second mode of operation, would make obvious to include other mode of operations to the CPU based on the mode register including the CPU and the clock pulse generator halt operation in one mode of operation.

17. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

Sato et al. (4,355,389) ; Akao et al. (US 5,307,464); and Ikeda (US 5,504,908).

18. **THIS ACTION IS MADE FINAL.** Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

19. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Nabil M. El-Hady whose telephone number is (571) 272-3963. The examiner can normally be reached on 9:00 - 4:00.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Bunjob Jaroenchonwanit can be reached on (571) 272-3913. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

January 24, 2006

Nabil El-Hady, Ph.D, M.B.A.
Primary Examiner
Art Unit 2152